UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,703	08/05/2003	David B. Glasco	NWISP036	8389

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EXAMINER
THOMAS, SHANE M

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/635,703	GLASCO, DAVID B.
	Examiner	**Art Unit**	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE **3** MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *2/17/2005*.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

This Office action is responsive to the amendment filed 2/17/2005. Claims 1-20 are

presented for examination.

All previously outstanding objections and rejections to the Applicant's disclosure and

claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Information Disclosure Statement

The IDS filed 2/17/2005 has been considered by the Examiner, and a signed copy has

been attached.

Drawings

The drawings included in the original filing, 8/5/2003, are now accepted by the

Examiner, as the previous objection of the brief descriptions of figures 10-15 have been removed

from the Applicant's disclosure.

Specification

As written, claim 20 invokes **35 U.S.C. 112, sixth paragraph**. If the Applicant does not

wish the claim limitation to be subject to this provision, claim 20 should be rephrased

accordingly.

Response to Arguments

Applicant's arguments regarding claims 1,5,11,15, and 20, filed 2/17/2005 have been

fully considered but they are not persuasive.

Applicant's arguments on pages 6-7 regarding claims 1,11, and 20, state that neither Hum

nor Webb teach a --completion response-- as recited in independent claims 1,11, and 20. The

Applicant further states, "In one example, the completion response is a completion bit provided

with response information." While Hum and Webb may not teach a completion bit per say, such

a --bit-- is not claimed, solely a --completion indicator--. The aforementioned claims recite only

"providing response information with a completion response to the processor." No limitation is

The Examiner, using a broadest reasonable interpretation for the claimed limitation interprets the

--completion indicator-- to be any means to *indicate* to the processor that the given transaction

(data requested in the case of Hum) has *completed*.

Hum teaches such a completion indication with the ACK message that is sent to the agent

120 to its [requesting] processor. The ACK message indicates to the processor the *completion* of

the data request (i.e. that the requested data has been sent), thereby making the ACK message a -

--completion indicator--. Again, while a Hum may or may not teach sending a --completion bit--

to the [requesting] process, such a limitation is clearly not present in the claims. As the

completion indicator appears to be a crux of Applicant's invention, as argued, the Examiner

recommends amending independent claims 1, 11, and 20 to further define the completion

indicator.

In addition, Hum may or may not teach that if a "completion [response] is not provided

that a requesting processor expecting responses from other nodes in a system," as such argued by

the Applicant on page 6, ¶3. Such a limitation is not found in independent claims 1,11, and 20,

thus the argument is rendered moot.

Applicant states on page 7 of the Response, "the acknowledge message does not provide

any completion indicator *as recited in the claims*. Providing a completion bit *as recited in the*

claims allows ...". Such a limitation is not present in independent claims 1,11, and 20; the

claims merely recite the providing of a --completion response--, which is being interpreted by the

Examiner to be any response received by the processor that indicated some form of the

completion of a request, as discussed above.

The Applicant argues on page 7 of the Response regarding the Webb reference

"providing responses from processors containing the request shared data line is not a completion

response. Once again, using the broadest reasonable interpretation of a --completion response--,

the Examiner disagrees. Webb teaches in column 6, lines 19-30, that before *completing* the

transition from shared to exclusive for a cache line, a processor must first receive a *response*

from processor 107 that indicates the number of shared copies of the cache line. This response

therefore indicates when the processor 100 may *complete* the transaction of transitioning the

cache line to the exclusive state. Therefore, it can be seen that the Examiner is regarding the

message retuned from the processor 107 to be a --completion response-- since in order to

complete the cacheline modification, a *response* must be sent to the requesting *processor*

regarding the *indication* of when the *completion* of the modification may take place. Thus Webb

anticipates independent claims 1, 11, and 20.

While Webb may or may not teach a --completion bit-- as previously mention by the

Applicant on pages 6 and 7, such a limitation is not present in argued claims.

Applicant argues with respect to claims 5 and 15 that "Neither Webb nor Hum teach or suggest any completion response that notifies the processor that the response from the cache coherency controller will be the only response." The Examiner disagrees. With regard to the Hum reference, the completion indicator from the cache coherence controller --notifies-- the receiving processor by indicating that the request data has been sent. Since the request by the requesting processor is satisfied with the data sent with the ACK message, the requesting processor does not expect another response. Thus the requesting processor is notified that the response from the cache controller is the only response because it *is* the only response expected from the coherence controller.

Additionally the prior art reference of Webb teaches a completion indicator that is sent from the data owner processor (i.e. directory processor - column 6, lines 15-30) where the response from the that --cache coherence controller-- is indicated to be the only response from the controller itself, as such is part of the cache-directory protocol. The protocol only requires a single response from the cache coherency controller, thus the notification that the completion response be the only response to the requesting processor is inherent as the requesting processor expects only a single response from the cache coherency controller.

As defined by the Examiner, the teachings of Hum and Webb *do* need a completion indicator. The completion indicator of Hum allows for the requesting processor to know when the request data has been sent, and the completion indicator of Webb allows for requesting processor to know the number of invalidations to wait for before modifying a cacheline, thereby preserve cache coherency throughout the point-to-point system.

To differentiate the prior art of record from Applicant's claims 5 and 15, the Examiner

recommends amending the aforementioned claims to indicate that the completion indicator that it

will be the only response *when more than one response [may be] is expect.* Such an amendment

would overcome the prior art of record, as Webb and Hum are silent with regard to a response

where the response bearing the completion indication is the only response when multiple

responses are expected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 11-17, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by

Hum et al. (U.S. Patent Application Publication No. 2004/0123047).

As per claims 1, 11, and 20, Hum teaches a method for providing a response to a cache

access request in figures 4 and 6. Further, Hum shows a *processing cluster* 110 in figure 1.

Figure 4 shows the receiving of a cache access request [that is associated with a memory line] at

a cache coherence controller (agent 120, figure 1). The cache coherence controller 120

represents multiple nodes, and cluster interface 210 (figure 2) provides two-way communication

between the agent 120 and the set of nodes (¶76). Since Hum states that an agent represents

multiple nodes (¶76), that a node can be comprised of a single processor (¶109), and that the

cache coherency system of the present invention is scalable (¶71), the Examiner is considering

elements 112-118 to be simple nodes (comprised of a single processor). Thus *cluster* 110

comprises cache coherence controller 120 and processor nodes 112-118. The processors of

cluster 110 are interconnected in a point-to-point architecture through agent 120 (refer to ¶¶ 55,

57 and 76). Response information for the cache access can be obtained from remote data cache

250 (import data cache) in accordance to figure 4 or can be obtained from remote data cache 260

(export directory) in accordance to figure 6. Since figure 2 is a representation of an agent (cache

coherence controller) is can be seen that remote data caches 250 and 260 are associated with a

given agent. In accordance with figure 4, the agent provides response information (step 450) to

the requesting node (processor). While not specifically mentioned in figure 4, a completion

response is sent along with the response information to the requesting node (processor). The

Examiner is considering the ACK message (¶44) to be a --completion response-- since it

indicates that the requested data has been sent to the requesting node (processor). While ¶42

states that the ACK message can be sent from the home node to the peer node, the Examiner is

considering the cache coherence controller 120 to act as the --home node--, or owner of the data,

when the cache coherence controller 120 fulfills a data request since the agent 120 can be

considered a node (representing its cluster of nodes - ¶63) and, therefore, must follow the cache

coherence process of the system (¶¶21- 46).

As per claims 2 and 12, the Examiner is considering the data response message from the agent 120 (cache coherence controller) that is sent to a requesting node (processor) to be a --response packet-- that comprises the requested data and the state of the data (M/E/F/S) to be used by the requesting processor (¶43).

As per claims 3 and 13, Hum teaches in ¶43 that in the cache coherency system of the present invention, state information (M/E/F/S) is included in the response information.

As per claims 4 and 14, as stated above, data is sent as part of the response information. Refer to ¶43 and figure 4, step 450.

As per claims 5 and 15, the Examiner is considering the ACK message that is sent from the agent 120 to one of its requesting nodes (processors) after the requested data to inform the requesting processor that that data response will be the *only response* to the data request since all data sent and received to a given processor (node) cluster of processors (nodes) is routed through the cluster's agent 120 (refer to figures1, 2, 3 and 5 and ¶64). It can be seen that the only response to a data request will be sent to the requesting processor's cache coherence controller (agent); thus, the reception of the --completion indicator-- (ACK message) indicates to the requesting processor that it will be the only response to the request. It follows, that since the request from the processor is satisfied, by the definition of the ACK message, another response will not be needed to be sent to the requesting processor.

As per claims 6 and 16, the Examiner is considering the node (processor) requesting the data to be a --requesting processor-- (for instance processor 112, figure 2), and the requesting processor's cluster (cluster 110) to be a --requesting cluster-- since the cluster comprised the processor from which a request for data initiated.

As per claims 7 and 17, as shown in figure 4, if the requested data is in the import cache (remote data cache) of the cache coherence controller, the data is forwarded to the requesting node (step 450). Only if the request misses in the remote data cache will the cache coherence controller (120) send the request to the nodes that are represented by the cluster (step 445). Thus, it can be seen that the ACK signal (completion indicator) that is sent by the cache coherence controller in step 450 allows the cache coherence controller from having to probe local nodes (step 445) or remote nodes (nodes connected to other braches of agent 190, for example).

Claims 1-7, 11-17, and 20, are rejected under 35 U.S.C. 102(e) as being anticipated by Webb, Jr. et al. (U.S. Patent No. 6,751,721), herein Webb.

As per claims 1,11, and 20, Webb teaches receiving a cache access request that is associated with a memory line at a cache coherence controller (directory processor 510, figure 5) from a requesting processor 500 in a cluster of processors 530. This access request is for exclusive ownership of the memory line in order to modify the line (column 5, line 62 - column 6, line 30). As shown in figure 5, the processors of cluster 530 are interconnected in a point-to-point architecture. Response information (data response from the directory processor containing the number of invalid responses that need to be received by the requesting processor before modifying the cache line) for the cache access request is received from a remote data cache associated with the directory processor 510 (cache coherence controller). The Examiner is

considering the cache of the directory processor to be a remote data cache since it contains a

share mask, which is responsible for maintaining the number of shared copies of a particular

cache line (column 6, lines 9-21). The Examiner is considering the --completion indicator-- to

be the number of invalid messages from processors containing the request shared data line.

Thus, in order to complete the modification of the cache line, the requesting processor 500 must

receive a certain amount of invalidate acknowledgements.

As per claims 2 and 12, the Examiner is considering the response to the requesting

processor 500 from the directory processor 510 (cache coherence controller) containing the

number of invalidate acknowledgements to be a response --packet--, data that is transferred from

processor to processor.

As per claims 3 and 13, the --completion indicator-- indicated --state-- information in that

it informs the requesting processor of how many *shared* cache copies exist in a system (such as

figure 3).

As per claims 4 and 14, the Examiner is considering a number value to be --data--.

Therefore, since the --completion indicator-- contains the number of invalidate

acknowledgements to be received before modifying a requested cache line, the response

information sent from the directory processor (cache coherence controller) to the requesting

processor contains --data--. Refer to column 6, lines 19-21.

As per claims 5 and 15, since the only response from the directory processor (cache

coherence controller) to the requesting processor is the number of current shared copies of the

cache line that are currently shared in the system, the requesting processor inherently knows (As

part of the system protocol) that the --completion indicator-- informs the requesting processor

that it will be the *only response* from the cache coherence controller (directory processor).

As per claims 6 and 16, the Examiner is considering the cluster 300 of figure 3 to be a

request cluster since it contains the processor requesting exclusive access to a memory line. As

can be seen, the processor 310 is a --requesting processor--.

As per claims 7 and 17, Webb teaches in figure 5 that the cache coherence controller

(directory processor 510) and requesting processor 500 can be contained within the same node

530, and therefore, does not have to probe local nodes (nodes that are connected adjacently to

node 530 - such as the two nodes directly connected to node 300 in figure 3) or remote nodes

(the remainder of the nodes in the system that are not directly connected to node 530).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-10, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Hum et al. (U.S. Patent Application Publication No. 2004/0123047), as applied to claims 1-7, 11-

17, and 20, above, in view of Keller (U.S. Patent No. 6,728,841).

As per claims 8 and 18, Hum does not specifically teach the [requesting] processor

sending a --source done-- upon identifying the completion indicator in the response from the

cache coherency controller. Keller teaches in column 2, line 63 - column 3, line 11, that a step of

sending a --source done-- upon receiving a response packet (including requested data) from a

target node. The source done response allows the target node to remove the request for data

from its command queue and can proceed to process the next request for the memory location.

As evidenced by Keller, the sending of the acknowledgement (source done) from the source

node back to the target node allows a cache coherent multiprocessor system to process memory

read requests effectively. Therefore, it would have been obvious to one having ordinary skill in

the art at the time the invention was made to have combined the cache response method of Hum

with the messaging response teaching of Keller in order to have effectively maintained cache-

coherence during memory reads in the multiprocessing system of Hum (figure 1 for instance). It

would have been seen by one having ordinary skill in the art that once the requesting node of

modified Hum (source node of Keller) received the read response (containing requested data)

followed by an ACK message (completion indicator) from the remote data cache (import cache

250) of the cache coherence controller (agent 120), the requesting processor (node) would have

sent a --source done-- response back to the cache coherence controller so that the cache

coherence controller could have removed the read request from its command queue and to

proceed to grant the subsequent next read request.

As per claims 9 and 19, as discussed in the rejection for claims 8 and 18, the --source

done-- message is sent to the cache coherence controller (agent 120).

As per claim 10, as discussed in the rejection for claims 8 and 18, the --source done--

response is sent back to the cache coherence controller (agent 120). The Examiner is considering

the cache coherence controller to be --acting as a memory controller-- since it controls the read

requests send to a node in its local cluster and can forward the data back to the requesting node

without having to send the request to the target node (processor). Refer to ¶63.

Claims 8-10, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Webb, Jr. et al. (U.S. Patent No. 6,751,721), as applied to claims 1-7, 11-17, and 20, above.

As per claims 8 and 18, Webb does not specifically show the requesting processor

sending a --source done-- message upon receiving the --completion indicator-- (number of

invalidations) in the response from the directory processor (cache coherency controller).

However Webb does state that the directory processor maintains a share mask register for each

cache line with bits indicating existing shared copies (column 6, lines 9-19). Since the

invalidation acknowledgement are sent directly to the requesting processor rather than to the

directory processor (column 6, lines 31-44), it would have been obvious to one having ordinary

skill in the art at the time the invention of Webb was made to have modified the invalidation

system of Webb to have sent a --source done-- response back to the directory processor (cache

coherency controller) after the requested cache line was modified by the requesting processor

(after receiving all the invalidation ACKs) in order to have informed the directory processor to

change the share mask of the corresponding cache line to indicate the cache line has been

modified by the requesting processor and is no longer being shared. In other words, the bit of the

corresponding shard mask would all be inactive. It follows that the --source done-- would have

occurred *after* the completion indicator - number of required invalidation ACKs - since the

requesting processor can only modify the cache line *after* receiving the correct number of

invalidation ACKs (column 6, lines 27-30). Such a modification to Webb would have

maintained cache coherence in the system by assuring that incorrect sharing information would not have been registered in the share mask of the directory processor.

As per claims 9 and 19, as discussed in the rejection of claims 8 and 18, the --source done-- message would have been sent to the cache coherence controller (directory processor) since the cache coherence controller maintains the share mask information that becomes updated when a cacheline is no longer shared.

As per claim 10, as discussed in the rejection of claims 8,9,18, and 19 above, the --source done-- message would have been sent back to the cache coherence controller (directory processor). The Examiner is considering the cache coherency controller to be --acting as a memory controller-- since it owns [and is responsible for maintaining share mask information for] the memory line (cacheline) that is being requested. Since it can be seen that the cache coherence controller *controls the memory* of the cache line, the cache coherence controller --acts-- like a memory controller.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas   HONG CHONG KIM
                         PRIMARY EXAMINER